LINEAR TECHNOLOGY

DESIGN NOTES

12-Bit 3Msps SAR ADC Solves Pipeline Problems

Design Note 192

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A new 12-bit 3Msps ADC brings unparalleled levels of performance and ease of use to the high speed ADC user. Its successive approximation (SAR) method eliminates many problems found in pipelined and subranging ADCs in that speed range. This note describes these problems and introduces a new, simple-to-use alternative, the LTC®1412.

The LTC1412 offers an ideal combination of speed, performance and size. Some of its features and benefits include:

- Complete low power 12-bit 3Msps ADC
- Great AC performance: 72.5dB SINAD and 83dB SFDR at Nyquist
- Great DC performance: ±0.25LSB typical INL and DNL (±1LSB max)
- Three-state output bus with no pipeline delay (parallel I/O with DSP interface signals)
- Tiny 28-lead SSOP package

PIPELINE PROBLEMS

Pipelined ADCs are great for giving the fastest speed short of that provided by a full-flash converter. In fact, LTC manufactures both pipelined and subranging ADCs. However, at resolutions of 12 bits and higher, these architectures can have a number of fundamental drawbacks. These drawbacks include poor noise and SNR, complex reference circuitry, complicated input circuitry, pipeline latency and poor frequency domain performance. These parts have large package size and high power dissipation. They also lack three-state outputs.

THE LTC1412 BENEFITS

The LTC1412's block diagram is shown in Figure 1. Some of the benefits offered by the LTC1412 SAR ADC design, when compared to pipelined ADCs, are discussed below. The August 1998 issue of *Linear Technology* magazine contains more information.

Benefit #1: Cleaner Behavior and Great Linearity

The LTC1412 depends solely on capacitor matching for accuracy (it has no pipeline amplifiers or interstage S/Hs with their resulting errors). This results in typical 0.25LSB INL and DNL that have virtually zero drift. Figure 2 shows the LTC1412's typical INL and DNL performance. Another benefit is freedom from sparkle codes, to which pipelined ADCs are susceptible.

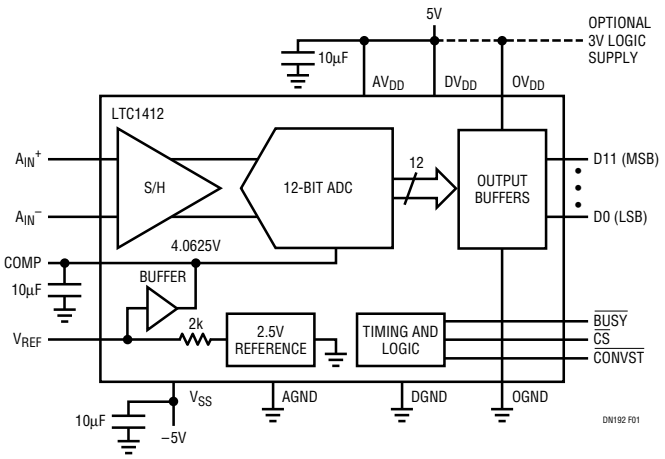

Figure 1. The LTC1412 Combines the Inherent Linearity of a High Performance 3Msps S/H and 12-Bit ADC with an Onboard Reference, µP/µC Logic Interface and Three-State Parallel Output Data Buffers

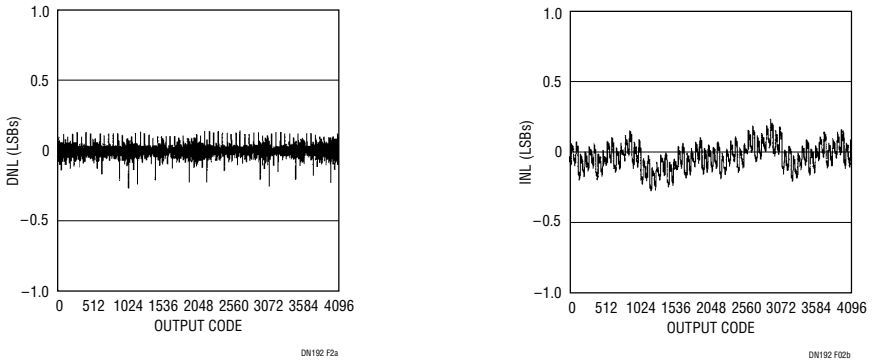

Figure 2 The LTC1412's Inherent Linearity is Shown in These INL and DNL Curves

Benefit #2: Lower Noise and Higher SNR

Pipelined ADCs add noise to their conversion because they resample the input signal as the conversion moves through the pipeline. Conversely, the LTC1412 has nearly perfect noise performance because its single S/H and single-pass conversion SAR architecture add almost no noise. This results in unsurpassed performance at 3Msps. Its 73dB (typ) SNR is within 1dB of the theoretical 12-bit ADC quantization noise. The LTC1412 also has premier distortion performance of 83dB spurious free dynamic range at Nyquist. Figure 3 shows an FFT of the LTC1412 at Nyquist.

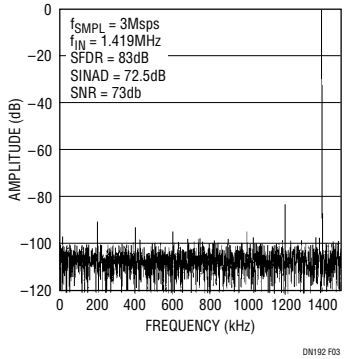

Figure 3. The LTC1412's Simple SAR Achieves 72.5dB SINAD and 83dB SFDR When Converting at 3Msps

Benefit #3: Simple Input and Reference Circuitry

The LTC1412's high impedance, differential input S/H and built-in reference greatly simplify analog support circuitry. The LTC1412's S/H eliminates the level shifting, complementary differential input signals or transformers typically required by pipeline ADC circuits. The LTC1412's reference does away with the multiple reference pins, multiple bypassing capacitors and fast reference buffer amps commonly required by pipeline converters. The LTC1412's internal reference maintains linearity over a 2:1 span adjustment voltage range. This flexibility covers a wide range of applications from communications to imaging.

Benefit #4: Easy Interface: Eliminates Pipeline Delay, Provides Three-State Outputs

Conversion data is present at the LTC1412's three-state output 300ns after the conversion begins, eliminating the pipeline delay, or latency, between the input sample and the corresponding output data. Having no pipeline, the LTC1412 does not suffer from time delay or phase shift, making it the choice in applications such as high speed servo-loop control systems and DSP, motor control, asynchronous or event-driven sampling and multiplexing.

Benefit #5: Small Package Size and Low Dissipation

While equaling the 3Msps pipeline ADCs' speed, the LTC1412's simple, efficient design and low power dissipation (150mW) allow small 28-lead SSOP surface mount packaging. This is much smaller than the packages used for pipeline ADCs, which can be as large as 44-lead PLCCs. Figure 4 compares the size of packages used for various pipeline ADCs and the SSOP packaged LTC1412.

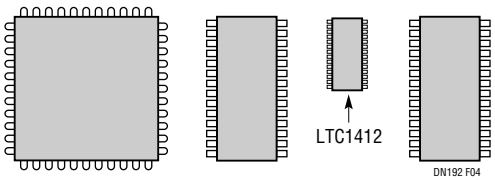

Figure 4. A Benefit of the LTC1412's Size and Power-Efficient Architecture is the Smallest Package Among 3Msps Parallel Output ADCs

Conclusion

Pipelined ADCs are useful at very high sample rates but they do have problems, as we have seen. Now, designers using pipelined 3Msps converters have a clean SAR alternative: the LTC1412. It is a sure cure for pipeline drawbacks and problems.

For literature on our A/D Converters, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 2453

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